EXHIBIT A

Disclosure of Expert Testimony for Dr. Thomas W. Dyer.

Introduction

The United States hereby provides notice of its intent to elicit expert testimony at trial in its case in chief from Dr. Thomas W. Dyer under Rules 702, 703, and/or 705 of the Federal Rules of Evidence. This disclosure is made pursuant to Rule 16(a)(1)(G) of the Federal Rules of Criminal Procedure.

The United States asked Dr. Dyer to review the technical material at issue in this case and determine (1) whether the information the government alleges the defendants stole from Micron satisfies the definition of "trade secret" in 18 U.S.C. § 1839(3), and (2) whether the defendants used information belonging to Micron—including trade secrets—to develop their own DRAM technology, and if they did, the extent and nature of that use.

The government hereby reserves the right to supplement this Notice as warranted. Pursuant to Criminal Rule 16(b)(1)(C), the Government requests that the defendant disclose any testimony that it intends to use under Rules 702, 703, and/or 705 of the Federal Rules of Evidence as evidence at trial.

Dr. Dyer's Qualifications

Dr. Dyer is an expert in dynamic random access memory ("DRAM") process technology, among other fields. Dr. Dyer earned his undergraduate Bachelor of Science degree in Physics and Mathematics with highest honors from the University of California at Riverside. He earned his Master of Science degree and Doctor of Philosophy (Ph.D.) degrees in Physics from the University of California at San Diego.

After post-doctoral research, Dr. Dyer worked at Los Alamos National Laboratory and Rockwell Semiconductor. At Rockwell, Dr. Dyer developed dielectric CVD processes for semiconductor manufacturing and performed materials characterization on advanced dielectric technologies.

After his semiconductor work at Rockwell, Dr. Dyer joined IBM's Semiconductor Research and Development Center in Hopewell Junction, New York as a Semiconductor Process Integration Engineer. Dr. Dyer spent 15 years with IBM, where he was involved in all aspects of process integration and served in various capacities from individual process module owner to overall integration leader for embedded DRAM technologies. Dr. Dyer helped develop seven CMOS technology nodes ranging from half-micron to 14 nm. His responsibilities spanned the entire process flow from front-end-of line processing for the fabrication of semiconductor devices, to back-end-of-line processing for building the copper wiring levels for interconnecting the devices, and to three-dimensional integration for the stacked integration of multiple circuit layers. Dr. Dyer participated in several DRAM, bulk CMOS, SOI CMOS, and SOI eDRAM

technology alliances involving various industry partners including Toshiba, Siemens, Freescale Semiconductor, Advanced Micro Devices, and GlobalFoundries.

At IBM, Dr. Dyer worked on all aspects of device fabrication. He developed deep trench capacitor and shallow trench isolation processes for quarter-micron through 90 nm DRAM technologies and optimized device structures and performance in 90 nm and 45 nm CMOS technologies. He designed and developed advanced CMOS DRAM process modules for trench capacitor, shallow trench isolation, gate stack, and contact levels. He led the introduction of high-k dielectric and metal electrode materials into embedded DRAM trench capacitors at 32 nm to replace the conventional silicon nitride dielectric and doped polycrystalline silicon electrode that had been in use for over a decade. In doing so, Dr. Dyer resolved several technology challenges to achieve the capacitance and leakage requirements, resolve thermal and dielectric stability issues, and integrate the new materials into the embedded DRAM fabrication process. By implementing those new materials, Dr. Dyer met capacitance and leakage specifications while simultaneously relaxing the aspect-ratio requirements of deep trench structure and dramatically simplifying the overall integration of the embedded DRAM capacitor.

Dr. Dyer left IBM in August 2013 for a position as Process integration Project Manager with SEMATECH's Process Technology Division in Albany, New York. There, he managed projects to develop advanced measurement techniques for advanced semiconductor manufacturing and developed integrated process flows for structures and devices used for strategic metrology and process equipment business opportunities. He worked closely with the business development teams to identify and develop Associate Member project prospects and worked with advisory groups across internal divisions to develop Core Member project proposals. He developed project plans and coordinated the activities and resources of SEMATECH, SUNY-CNSE, and member companies to meet project objectives. He established a III-V Center for Excellence at Albany's Center for Semiconductor Research (CSR) where he coordinated activities of various Albany Nanotech tenants to establish III-V processing infrastructure, leveraged SEMATECH and CSR resources for III-V business opportunities, developed and managed III-V process integration projects, and worked with the Environmental, Health, and Safety department to address EHS risks of III-V processing. When SEMATECH was acquired by the State University of New York College of Nanoscale Science and Engineering in August 2015, Dr. Dyer transferred to the Photonics Integration Group to serve as a custom photonics project manager. There he developed new process technologies for visible-light photonics application such as displays for augmented-reality eyewear.

Based on his work at IBM, Dr. Dyer is the named inventor of 94 issued U.S. patents for inventions in the field of semiconductor processes, structures, and devices. Thirteen of those patents relate to DRAM and embedded DRAM processes and structures. Dr. Dyer served on IBM's Invention Development Team for 14 years where he reviewed and evaluated thousands of inventions covering device structures and methods of fabrication for novelty, technical merit,

usefulness, and potential business impact. IBM recognized Dr. Dyer as an IBM Master Inventor in 2012.

Dr. Dyer's further qualifications are described in his *curriculum vitae* is attached as Exhibit 1. The government has compensated Dr. Dyer for his time at a rate of $375/hour.

Summary of Methodology

Dr. Dyer's work consisted primarily of reviewing documents and applying his knowledge, training, and expertise in the field of semiconductors, semiconductor fabrication processes, and DRAM to interpret the meaning of those documents and incorporate those documents into forming opinions about the topics requested.

Dr. Dyer began by reviewing Trade Secrets 2-8 and various other Micron documents provided to him by the government as documents the government alleges were stolen and possessed by engineers and managers, including the individual defendants, working on the UMC/Jinhua DRAM project known as "Project M." He subsequently received a copy of the hard drive known as Hard Drive 48 (aka, "the Taiwan Drive"), along with a description of the drive's contents, as a further source of stolen Micron documents relevant to Trade Secret 1. Dr. Dyer extensively reviewed the Micron documents to consider their meaning, value, the extent to which the information was in the public domain, and the ease with which a semiconductor company could reverse engineer the Micron information.

After familiarizing himself with the allegedly stolen Micron technology, Dr. Dyer reviewed numerous other sources of evidence related to the work performed for Project M. That evidence included all manner of technical, programmatic, and marketing documents related to Project M in the government's possession. Such documents included transcripts of interrogations provided by authorities in Taiwan, development documents, email communications among Project M participants, GDS files, technical presentations, spreadsheets, and documents obtained by the government from subpoenas and search warrants. The government provided Dr. Dyer with access to all documents produced by the government in discovery, including all documents obtained from Taiwan and pursuant to the government's cooperation agreement with United Microelectronics Corporation (UMC), so that he could perform his own searches for relevant documents he thought necessary to formulate his opinions.

Using his training and experience, Dr. Dyer compared the Micron and the Project M documents to identify similarities and differences. His comparisons were informed by Project M communications, statements of individuals involved in the project, and project planning documents. Based on all of that information and his substantial training and experience in the field, Dr. Dyer formed opinions about whether and how Project-M members used the stolen Micron information to advance the project, as well as how they deviated from the Micron technology and why.

Materials Considered

The government provided Dr. Dyer with access to its database of discovery documents in this case. Dr. Dyer also received a copy of the "Taiwan Drive," which the government received from authorities in Taiwan, and produced to the defense on July 8, 2020. Attached as Exhibit 2 is a list of documents Dr. Dyer reviewed from the government's database of discovery.

In addition to reviewing documents, Dr. Dyer spoke with various Micron employees in order to gather information and confirm his understanding of Micron documents he reviewed. The contents of those discussions are described in Exhibit 3.

Similarly, Dr. Dyer spoke with the government's foundry expert—Terry Daly—to provide information and explanations to Mr. Daly. The contents of that discussion are also described in Exhibit 3.

Summary of Expert Opinions

I. Foundational Concepts for Understanding DRAM and DRAM Manufacturing

Dr. Dyer will testify about certain foundational concepts related to DRAM and its manufacturing. Among these concepts, Dr. Dyer may explain:

- The flow of electrical current across positive and negative junctions;
- The "field effect" in which charge carriers in a semiconductor can be modulated by an externally applied charge;
- Metal-oxide-semiconductor ("MOS") structure, which is a simple structure for imparting the field effect in a semiconductor;
- Charge carrier modulation, in which the charge carriers in the semiconductor directly under the metal electrode can be modulated by varying the charge on the electrode;
- Two key electronic devices used in DRAM chips – namely, transistors and capacitors, including metal-oxide-semiconductor field-effect transistors ("MOSFETs"); and
- Integrated circuits, which are a collection of electronic devices formed on a single substrate and connected together.

Based on those concepts, Dr. Dyer will explain the scaling (shrinking) of integrated circuits in the six decades following their introduction. Dr. Dyer will describe the fabrication of today's integrated circuits on chips and wafers through manufacturing processes that requires hundreds of steps arranged in a precise sequence, with carefully formulated recipes and

sophisticated tools in expensive, automated fabrication facilities called "fabs." Dr. Dyer will discuss the deposition, removal, doping, and patterning stages of the manufacturing process.

Dr. Dyer will describe the design of and design rules for modern integrated circuits. He will discuss the similarities of and differences between logic and memory chips, in particular DRAM memory chips. Although they are both semiconductor chips, logic and DRAM chips perform different functions and are subject to different requirements, which have in turn led to divergent structures, design methodologies, and fabrication techniques. Among other differences, Dr. Dyer will explain the emphasis on density in DRAM chips and how density has caused DRAM manufacturers to use of specialized structures, such as recessed transistors and stacked capacitors.

Dr. Dyer will show one or more schematics of DRAM chips. DRAM cells are arranged in a two-dimensional matrix. One side of each cell transistor is connected to the capacitor in that cell. The other side is connected to a wire that runs across the entire array in one direction and also connects to the transistor of every other cell in that row of the array. Such a wire is used in each row of the DRAM cell in the array, in parallel lines running across the array. Those wires are called "bitlines" or "digitlines." Another set of wires runs perpendicular to the bitline and across each column of the array. Those wires are connected to gates of the transistors in each cell in that particular column. Those wires are called "wordlines." An entire row of memory cells is accessed simultaneously when the corresponding wordline is activated. Most of the wiring in a DRAM chip is accomplished with those two wiring levels. DRAM chips also contain a relatively small amount of logic circuitry in the peripheral regions outside of the array. Those areas are small compared to the arrays and have relatively little impact on the overall size and density of a DRAM chip.

In contrast to DRAM, which has large, dense, and regularly laid out arrays of memory cells, logic chips seek transistor performance and interconnectivity, the latter of which has led to more than ten separate layers of metal wiring in modern logic chips. The different design considerations between DRAM and logic, and the associated structural differences—for example, long recessed transistors in DRAM to minimize leakage and maximize retention compared to shorter transistors in logic chips to promote fast switching—drive different manufacturing processes and requirements to develop different manufacturing technology. With transistors, for example, the DRAM manufacturing process will include steps to recess the silicon to form the notch for the recessed transistor, while the logic process will not. Similarly, the DRAM manufacturing process will include steps to form the gate insulator and buried gate conductor inside the notch to minimize off-state current leakage and maximize array density. The logic process will not.

II. The Information Identified as Trade Secrets 1-8 in the Indictment Meet Elements of the Definition of "Trade Secret" in 18 U.S.C. § 1839(3)

Dr. Dyer's testimony will describe the information labeled in the Indictment as Trade Secrets 1-8. Dr. Dyer will describe the technical meaning of the information composing each of Trade Secrets 1-8. Dr. Dyer will further describe the technical challenges that must be overcome to develop the information compiled in Trade Secrets 1-8, the complexity of those challenges, and the resources required to solve them.

Dr. Dyer's explanations will be based on his technical training and over 25 years of experience working in the field of semiconductors and process integration. Through that experience, Dr. Dyer has become familiar with the technologies and scientific principles behind those technologies. That familiarity enables him to interpret documents describing semiconductor design and manufacturing processes. Dr. Dyer also has experience reviewing technical documents of the same type as those composing Trade Secrets 1-8. He is therefore well positioned to review Trade Secrets 1-8 and apply his knowledge to interpret and describe their technical content to a lay jury.

Through his industry experience and academic research, Dr. Dyer also has experience with the nature and complexity of the scientific and engineering effort required to develop the information in Trade Secrets 1-8. He thus understands the scope of the technical effort required to develop such technology, including the resources that must be invested in order to develop such technology and information. Dr. Dyer's experience in the industry also has allowed him to understand how companies engaged in DRAM manufacturing typically develop or acquire DRAM technology, given the complexities involved. Dr. Dyer will apply the knowledge he has gained regarding these topics to offer opinions about the effort and resources required to develop the information in Trade Secrets 1-8.

A. Trade Secret Descriptions

Dr. Dyers's testimony regarding Trade Secrets 1-4 and 6-8 will primarily focus on the combination of steps, the sequence of steps, the combination of step recipes, and/or the combination of tools Micron used to implement the process steps—all as described in each of Trade Secrets 1-8—as comprising valuable trade secrets. Collectively, Dr. Dyer may refer to such trade-secret information as "steps, recipes, and tools." The steps, recipes, and tools for a particular Micron DRAM process are a trade secret considered in combination. Each, however, is separately a Micron trade secret. For example, Dr. Dyer will testify that each of following is independently a Micron trade secret (or meets the elements of the definition of "trade secret"): (1) the combination of process steps used to create Micron's 25 nm DRAM product; (2) the sequence of process steps used to create Micron's 25 nm DRAM product; (3) the combination of recipes used for the various process steps used to create Micron's 25 nm DRAM product; and (4) the combination of tools used to implement the process used to create Micron's 25 nm DRAM

product. Dr. Dyer will also testify that the sub-parts of each of the above identified in the government's forthcoming bill of particulars are trade secrets (or meet the elements of the definition of ("trade secret"). Dr. Dyer will offer similar testimony with regard to Micron's 20 nm (100 series) and 1x nm (110 series) DRAM, which constitute independent sets of trade-secret information.

1. **Trade Secret 1**: Dr. Dyer may testify that he has reviewed the information defined by as Trade Secret 1, which he understands to be the combination of information in Trade Secrets 2-8 along with the files in the table below, which Dr. Dyer understands to have been brought to Project M by Kenny Wang and/or JT Ho.

【DR25nmS】Design rules Periphery_EES_2012000026-013_Rev (version 1).xls
★★Elpida 25nm process flow_Modify.ppt
★★Elpida 25nm process flow_peri.ppt
dram_comparison_workshop_100-110_series.pdf
Elpida 25nm process flow.pdf
Template_Tool Mapping_Fab11_Fab16 110sD Tool Risk (F16)-0831 discussion.xlsx Template_Tool Mapping_Fab11_Fab16 110sD Tool Risk (F16)-0908.xlsx
R1 F72 1GC Flow0411 no defect.xls
R1 F72 1GC Flow0411 no defect_1.xls
Rexchip 25nm Flow summary _IMP & RTP.xls
Rexchip 25nm Flow summary 0614 CMP.xls
Rexchip 25nm Flow summary 0614 Diff.xls
Rexchip 25nm Flow summary 0614 Photo.xls
Rexchip 25nm Flow summary 0614 wet.xls
Rexchip 25nm Flow summary 0710 TF.xls
F32 2014,2015 flow compare-20180824.xlsx

Dr. Dyer may testify that he considers the Micron files that constitute Trade Secret 1 to be representative of the totality of Micron information on the drive known as "Hard Drive 48," which Dr. Dyer understands to contain files found on various digital devices owned by JT Ho, Kenny Wang, and others.

Dr. Dyer may testify that the Trade Secret 1 includes extremely detailed information regarding the process to manufacture DRAM. Trade Secret 1 is a complete description of virtually every important aspect of Micron's DRAM manufacturing processes for multiple technology nodes, including, for example, process recipes, process steps, the sequence of process steps, implant conditions (a specific type of process step and recipe), and tooling.

In addition to Trade Secrets 2-8, described below, Dr. Dyer may testify about information in the other files that constitute Trade Secret 1 as follows:

- 【DR25nmS】Design rules Periphery_EES_2012000026-013_Rev (version 1).xls – This is another file that contains Micron's design rule information, as further described in Trade Secret 5.

- ★★Elpida 25nm process flow_Modify.ppt – This is an Elpida version of the 25 nm process flow, that includes a step-by-step description, with diagrams of the manufacturing process. The Elpida 25 nm process evolved into the Micron 25 nm process after Micron acquired Elpida.

- ★★Elpida 25nm process flow_peri.ppt – This document contains essentially the same information as the document described above.

- dram_comparison_workshop_100-110_series.pdf – This document contains a lot of the same information as in Trade Secrets 6-7. The document appears to include material to train Micron engineers on the differences between the 100 and 110 series DRAM at Micron.

- Elpida 25nm process flow.pdf – This is an earlier version of the Elpida 25 nm process flow described above.

- Template_Tool Mapping_Fab11_Fab16 110sD Tool Risk (F16)-0831 (and -0908) – This is a spreadsheet describing as-installed process details, including a tool list, for Micron's Fab 16.

- R1 F72 1GC Flow0411 no defect.xls – This is spreadsheet describing detailed process information and comparisons for the Elpida and Rexchip fabs.

- R1 F72 1GC Flow0411 no defect_1.xls – This is spreadsheet describing detailed process information and comparisons for the Elpida and Rexchip fabs.

- "Rexchip 25nm Flow Summary" Documents – This document family contains a very detailed, step-by-step listing of the operations, tool vendors and types, recipe parameters (including temperatures, pressures, RF powers, gas-flow rates, etc.) for Micron's DRAM 25 nm DRAM process at Fab 16. The document has all of that process information for two different 25 nm DRAM products and for two wafers fabs—the Rexchip R1fab (became Micron Fab 16) and the Elpida E300 fb (became Micron Fab 15). The documents contain a degree of detail that would allow a wafer fab to install an essentially exact version of the Micron process in a different fab equipped with a similar set of tools as specified in the process spreadsheet. Different versions of the spreadsheet are filtered to reflect different parts of the DRAM manufacturing process:

    - Rexchip 25nm Flow summary _IMP & RTP.xls – This is a version of the Rexchip process flow described above that has been filtered to focus on implant and rapid thermal processing (RTP) process steps.

- Rexchip 25nm Flow summary 0614 CMP.xls – This is a version of the Rexchip process flow described above that has been filtered to focus on chemical mechanical planarization process steps.

- Rexchip 25nm Flow summary 0614 Diff.xls – This is a version of the Rexchip process flow described above that has been filtered to focus on thermal diffusion process steps.

- Rexchip 25nm Flow summary 0614 Photo.xls – This is a version of the Rexchip process flow described above that has been filtered to focus on photolithography process steps.

- Rexchip 25nm Flow summary 0614 wet.xls – This is a version of the Rexchip process flow described above that has been filtered to focus on wet-chemistry process steps.

- Rexchip 25nm Flow summary 0710 TF.xls – This is a version of the Rexchip process flow described above that has been filtered to focus on thin-film deposition process steps.

- F32 2014,2015 flow compare-20180824.xlsx – This document includes process information, including process steps and sequences, for Micron's 25 nm process flow. The document does not contain the same level of recipe information as the Rexchip 25 nm Flow Summary (for two products at both the Micron Fab 15 and Fab 16), but includes more recent / updated process information from Micron dated August 2014 and August 2015.

2. **Trade Secret 2**: Dr. Dyer will testify that Trade Secret 2—a file called "Fab90s Traveler-20150518.pdf"—is a process traveler document for Micron's 90 Series DRAM process, which has a 25nm feature size. A traveler document is a descriptive document that describes the process flow for creating Micron's 25 nm DRAM product. The traveler document describes the sequence of steps that make up the process flow, typically along with a brief description of the process parameters—or recipes—Micron uses for each step. The traveler document typically describes multiple process steps on each page, and includes references to Micron's internal naming conventions for each process step. The document includes detailed illustrations with cross-sectional and three-dimensional views of DRAM structure at over 100 different points throughout the process sequence.

3. **Trade Secret 3**: Dr. Dyer will testify that Trade Secret 3—a file called "[redacted] (ALL) IMP conditions Table_20150318.xlsx"—is a detailed description of the ion implant conditions used to form electrical devices that are the components of the various circuits used to create a DRAM chip. Ion implantation involves "shooting" atoms into the silicon—or adding "dopants"—to modify the electrical behavior of the silicon in defined areas. Trade Secret 3 contains detail on the ion implant process steps in Micron's 25 nm process technology. The first few tabs of the spreadsheet contain tables describing the photolithography masks used for the ion implant steps.

The tables in the document describe various transistor types, and the implant conditions that apply to each. The next few tabs contain the detailed parameters for each ion implant including the species, dose, energy, and other information for multiple products within the 25 nm technology series.

4. **Trade Secret 4**: Dr. Dyer will testify that Trade Secret 4—a file called "[redacted] Implant Condition for MES setting_1015.xlsx"—also describes ion-implant conditions for Micron's 25 nm technology. Many of the explanations that apply to Trade Secret 3, therefore, also apply to Trade Secret 4. The spreadsheet includes Micron' ion-implant for multiple products. The file includes the software parameters used with the manufacturing execution system (MES) that manages ion implants on the fabrication line.

Dr. Dyer will testify that the ion-implant information in Trade Secret 4 is even more valuable than the information in Trade Secret 3 because it contains a more complete set of ion-implant recipe parameters. The file provides separate tables for different 25 nm DRAM: high performance and low power.

5. **Trade Secret 5**: Dr. Dyer will testify that Trade Secret 5—a file called "【DR25nmS】Design rules Periphery_EES_2012000026-013_Rev.13.xls" is design rules for the memory cell, array and peripheral areas of Micron's 25 nm process technology, dated 2/9/2016. The file contains tables listing hundreds of design rules for Micron's (formerly Elpida's) 25 nm process technology. The sheet in each tab is labeled "Micron Technology, Inc. Confidential and Proprietary."

Dr. Dyer will describe that design rules describe the constraints within which circuit designers must design their integrated circuits, in order for those circuits to be manufacturable at a particular fab. Design rules are specific to a particular fab and process. A fab provides its design rules to circuit designers (e.g., fabless circuit-design companies). The circuit designers will design and layout their circuits to conform to the design rules, in order to ensure that the fab will be able to manufacture their design.

6. **Trade Secret 6**: Dr. Dyer will testify that Trade Secret 6—a file called "DRAM_100_series_(20nm)_traveler_(v00h) 150730.pdf"—is a process traveler document for Microns 100 Series DRAM process, which has a 20 nm feature size. As described for Trade Secret 2, the Trade Secret 6 contains the process steps and sequence—with some recipe information for the various steps—for Micron's 20 nm DRAM technology. Every page of the document is designated as Micron confidential.

The document contains background information for Micron's 20 nm process technology, including a technology comparison table that contains key dimensions of Micron's DRAM cell and diagrams showing how the different layers of those cells are laid out. Beginning on page 20,

the document contains a detailed illustration of the entire fabrication process from start to finish, with descriptions of the hundreds of individual steps. The descriptions of the process steps include detailed illustration showing three-dimensional and cross-sectional views of the DRAM structure at over 100 different points throughout the process sequence. Accompanying the illustrations are step descriptions including the purpose of each step along with other information about the process.

A technology is often referred to by its minimum dimensions. For example, the active area spacing in a 3x2 DRAM technology is the minimum dimension of the layout. For a "25 nm technology" this dimension is 25 nm. That is where the 25 nm comes from in "25 nm technology."

The technology can also be described by an "average" feature size instead of the minimum feature size. A way to calculate this "average" for a 6F2 cell is to divide the cell area by 6 and take the square-root of the result. For a 25 nm technology with cell dimension of 80x78, this gives 32 nm. That is where the 32 in "F32" comes from.

7. **Trade Secret 7:** Dr. Dyer will testify that Trade Secret 7—a file called "dram_110_series_(1xnm)_traveler_(z11a)-20150915.pdf"—is a process traveler document for Microns 110 Series DRAM process, which has a 1x nm feature size. As described for Trade Secret 2, the Trade Secret 7 contains the process steps and sequence—with some recipe information for the various steps—for Micron's 20 nm DRAM technology. The traveler document typically describes multiple process steps on each page, and includes references to Micron's internal naming conventions for each process step. The document includes detailed illustrations with cross-sectional and three-dimensional views of DRAM structure at over 100 different points throughout the process sequence.

"1x" represents a number between 10 and 19 and describes the first technology node for a DRAM company that comes after 20 nm. Every page except the last two are labeled as Micron Confidential. The document includes a technology comparison table that contains the key dimensions of Micron DRAM cells and diagrams showing how different layers of cells are laid out. Page 24 describes how Micron's 1x nm cell layout shifts from the 2x3 cell layout used in the 20 nm and earlier technology nodes, to a 3x2 cell layout. In a 3x2 layout, the active area features are more tightly spaced, but the wordline spacing is more relaxed than a 2x3 layout. The active areas are interlaced in 3x2 layout, but are lined up evenly in the 2x3 layout.

The document further explains motivation for changing from a 2x3 layout to a 3x2 layout. Micron moved to a 3x2 layout to alleviate row-hammer issues. "Row hammer" describes an undesirable mechanism within DRAM whereby information stored in one memory

cell can change when a nearby row is accessed repeatedly (i.e., hammered). Relaxing the wordline spacing with the move to a 3x2 layout helps alleviate the row-hammer mechanism.

8. **Trade Secret 8:** Dr. Dyer will testify that Trade Secret 8—a file called "dram_1xnm_process_(Z11AA41200)_-_summary_flow_document.pdf"—is a Process Summary Flow Document for Micron's 110 series (1x nm). The document is an earlier version of the document described for Trade Secret 7, and contains the same type of information as Trade Secret 7. Dr. Dyer's testimony for Trade Secret 8, therefore, will mirror that of Trade Secret 7.

Dr. Dyer will testify that Trade Secret 8 has errors that were corrected in Trade Secret 7. Additionally, Trade Secret 7 reflects a small number of minor process changes as compared to the process described in Trade Secret 8. One difference that was notable was in the technology comparison tables in Trade Secret 7 and Trade Secret 8. All of the cell parameters for each of the technology nodes are exactly the same (as expected), except for the AA angle (active area angle). The AA angle for the 1x nm node is listed as 21.05° in Trade Secret 7 and 20.6° in Trade Secret 8. The geometric calculation of the AA angle, based on the wordline half-pitch of 26.5 nm and a digitline (bitline) half-pitch of 30.6 nm yields a AA angle of 21.05°. This indicates that 20.6° may be an erroneous statement of the AA angle, at least as far as the geometric relationships are concerned with calculating the average angle over the entirety of the array.

B. The Information in Trade Secret 1-8 is Not Generally Available in the Public Domain

Dr. Dyer will testify that the information comprising each of Trade Secrets 1-8 (including the subparts identified in the government's forthcoming bill of particulars) is not generally available in the public domain. Specifically, the combination of steps and their sequence, combination of recipes used for the steps, and the combination of tools used to accomplish the steps are not generally available in the public domain. That opinion is based on Dr. Dyer's extensive training and experience working on semiconductor process integration and DRAM technology, especially at IBM and SEMATECH. That experience has allowed him to gain an understanding of (1) the type of design and process-technology information that semiconductor companies do not make publicly available and (2) the type of information that generally exists in the public domain regarding DRAM design and process technology.

Dr. Dyer will testify that the semiconductor companies that develop technology generally have three ways to treat the information: to publish it, to file for patent protection of it, or keep it as a trade secret. Dr. Dyer will testify that a company's choice affects its ability to freely use that new technology to its advantage and to restrict others from using it.

Dr. Dyer will testify that a decision to publish means disclosing the information in a public form. Publishing the information gives the company an unencumbered right to use the

technology disclosed, while preventing others from patenting the technology and thereby acquiring exclusive rights to it. Publishing the information, however, does not prevent others from freely using the information. A semiconductor company generally publishes information or technology that that wants to use itself, but does not see an advantage in restricting others from using it. Publishing information costs very little and gives the company the right to use the information as needed, without the threat of someone else trying to claim it and restrict the company from using it. Technology that could be useful, but probably not worth the cost of pursuing patent protection, would typically be a good candidate for publication.

Dr. Dyer may testify that the decision to file for patent protection is typically made for information that is valuable and might be discoverable in a final product. In semiconductors, structural features that are discoverable or observable in the final product are good candidates for patent protection. That is both because (1) a competitor would be able to observe or determine the nature of the technology and (2) the company would be able to detect or observe use of its patented technology in a competitor's products, and seek the appropriate relief. In semiconductor companies, fabrication methods are generally not good candidates for patent protection since they generally do not leave traces that can be seen in the final product and one would not know whether or not a competitor was using the same method of fabrication as claimed in a patent.

Dr. Dyer will further testify that fabrication methods tend to be good candidates to be kept as trade secrets because of their generally undiscoverable nature. That includes process steps, the sequence of process steps, the parameters or recipes used at each process step, and the tools (or combination of tools) used to accomplish the process steps.

Dr. Dyer will testify that much of the information in Trade Secrets 1-8 have the characteristic of this third category and are classic examples of information that a semiconductor company would keep as trade secret, instead of publishing or seeking patent protection.

Dr. Dyer will testify that Mr. Bissy has confirmed that Micron's approach to handling intellectual property is similar to what Dr. Dyer has described.

Dr. Dyer's opinions in this section are based on his extensive training and experience working in and with semiconductor companies. Dr. Dyer also performed reasonable public-domain searches to determine that the information the government claims is a trade secret does not exist in the public domain. Additional, Dr. Dyer has experience as a named inventor on 94 U.S. patents, issued because they disclosed inventions not in the public domain.

C. The Information in Trade Secrets 1-8 Is Not Readily Ascertainable Through Proper Means by a Person or Company Skilled in Semiconductors

Dr. Dyer will testify that the information composing each of Trade Secrets 1-8 (along with the subparts identified in the government's forthcoming bill of particulars) is not readily ascertainable through proper means by a person or company skilled in the field of semiconductors. Reverse engineering of completed semiconductors chips is extremely limited in determining the process (i.e., steps, recipes, and tools) by which those chips were made. In general, reverse engineering of a semiconductor chip can reveal the physical structure of a completed chip, but not the process steps used to manufacture the chip, the sequence of those steps, the recipes/parameters applied for each process step, or the tools used to complete each process step. Dr. Dyer will testify that it is impossible using modern technology to determine the steps, recipes, and tools (including ion implant conditions) described by the information in Trade Secrets 1-8 using reverse engineering.

Dr. Dyer will testify about reverse engineering techniques used to analyze integrated circuits. He will testify that there is a range of techniques use for analyzing the structure and material composition of the various features of the integrated circuits.

He will testify that optical microscopy is of very limited use in reverse engineering integrated circuits because the component parts of the devices and structures in an integrated circuit are much smaller than the wavelength of visible light. The physical features of the devices, therefore, cannot be resolved by visible light. Dr. Dyer will testify that the wavelength of the visible light is more than an order of magnitude larger than the minimum feature of a 25 nm technology.

He will testify that, instead of optical microscopy, electron imaging techniques are used to visualize the structures of integrated circuits. He will testify that there are two primary electron imaging techniques used: scanning electronic microscopy (SEM) and transmission electron microscopy (TEM)

He will testify that a SEM looks at the surface of a sample and provides monochromatic image of the surface features. A SEM can operate in different modes to either give detailed images that provide contrast between different materials present in the surface or to provide images that give a 3d-like perspective of the surface topography of a wafer. The contrast between different materials in a SEM can be enhanced by performing various types of surface treatments to the sample surface. Such techniques include, for example, (1) coating the surface with a thin conducting material to prevent negative charge build-up on the surface during imaging and (2) slightly etching the surface with a chemical that etches different materials at different rates to induce some topography and enhance the contrast between materials. The resolution of a SEM is typically about 10 nm.

Dr. Dyer will also testify that a TEM provides an image through the volume of a thinned sample. A typical TEM sample is about 100 nm thick. Preparing a TEM sample is labor intensive as it is difficult to get a sufficiently thinned sample in the targeted region of interest. The TEM provides monochrome images where the contrast is determined by the how easily the electron beam penetrates the different materials in the thinned sample. The lateral resolution of a TEM is greater than that of a SEM. A TEM can achieve atomic level resolution of a few tenths of a nanometer.

Both types of electronic microscopes can be used to obtain compositional information about the sample. The same electron beam that is used for imaging can be used to analyze the atoms making up the materials. The beam can be focused on a small spot and scanned across the sample to provide a two dimensional map of the material compositions.

Dr. Dyer may testify that the images obtain by SEM and/or TEM can be of different orientations through the samples depending on how the samples are prepared. For example, cross sectional information can be obtained by cutting the sample perpendicular to the top surface and then imaging it edge-on. These techniques can also provide a plane-view images at a given depth into the samples by de-layering the surface layers to a desired depth before imaging. That, however, can be an extremely labor intensive and costly technique.

Most of the information in a typical reverse engineering report for an integrated circuit will be SEM and TEM images due to the value of the pictorial representations they provide. Other techniques are also available to complement the images provided by electron microscopy. Those techniques can provide additional detail of the material composition, surface roughness, and electrical properties of the materials.

Dr. Dyer will testify that typical reverse engineering techniques can provide detailed structural information about microelectronic circuit features, but at a high cost. High resolution analysis of a single sample, for example, requires the use of specialized equipment and highly-trained personnel to operate it. The preparation of a sample required before imaging can be performed can be a very labor-intensive process in itself.

Dr. Dyer will testify that the structural information that can be obtained from reverse engineering is of limited value in determining the fabrication process used in manufacturing an integrated circuit. There are many ways that final structures of integrated circuits can be made that leave no trace of various of the steps, the overall sequence of steps, the exact process conditions for the various steps, or the use of intermediate sacrificial structures that may be used to assist in the construction of the final structure, but are removed from the final product after they serve their purpose in manufacturing. Dr. Dyer will testify that there are all kinds of tricks used in nanofabrication that cannot be deciphered by looking at the final structures. Similarly, reverse engineering provides limited information about the precise tools used in the manufacturing process.

Dr. Dyer will testify that it is impossible to determine the process parameters of the many individual steps that are used in microelectronics process flow. There is no way to determine the exact temperature, gas flow rates, process chamber configurations, chemicals and reactions used, surface modification techniques used, etc., in the manufacturing process. Such parameters can individually or in combination have a critical impact on the ultimate functionality of the integrated circuit. It is only through continual refinement, generation after generation, that the specific combination and specific details of the various process steps are able to yield functioning and reliable circuits.

Dr. Dyer may testify that the exact ion implantation conditions used to dope a semiconductor also cannot be determined through reverse engineering. Some information about an implant species can be obtained by secondary ion mass spectroscopy (SIMS) analysis of different regions of the chip, but those techniques are not able to resolve the small-scale implantation profiles of individual devices. Scanning capacitance microscopy could be used for higher resolution mapping of device dopant profiles, but would still fall short of giving precise enough information to pinpoint the exact ion implant conditions and the terminal diffusion conditions that used to produce the doped regions. Other details such as the implant angle (between the wafer surface and the ion beam), screening materials (e.g., oxides) through which silicon is doped by the ion beam, and pre-amorphization of the silicon surface all affect the implant profiles without leaving a clear trace of the exact process conditions used.

Dr. Dyer's testimony regarding reverse engineering and the legitimate means of acquiring DRAM process technology will be based on his extensive training and experience in DRAM and the broader microelectronics industry. This includes his experience working on behalf of the entire industry at SEMATECH. Dr. Dyer's testimony is also based on his own involvement and experience with reverse-engineering techniques during his career. Dr. Dyer will testify that, to his knowledge, semiconductor companies generally engage in reverse engineering or look at reverse-engineering reports of their competitors' products for competitive-analysis purposes, and are familiar with limitations of reverse engineering to decipher the details of a fabrication process. The limitation of reverse engineering are both fundamental—as many process details leave no trace of their existence, nature, and/or order in the sequence—and practical—as acquiring information from physical analysis can be very expensive. There are companies that specialize in reverse engineering advanced technologies of various manufacturers and sell the reverse engineering reports to competitors for thousands of dollars, and their reports only give detailed information on the final structures and are incapable of providing specifics about fabrication processes, steps/sequences, recipes, and tools.

D. The Information in Trade Secrets 1-8 Derives Independent Economic Value from Its Secrecy

Dr. Dyer will testify that the type of detailed process information in Trade Secrets 1-8 (including the subparts identified in the government's forthcoming bill of particulars) is considered highly sensitive and proprietary intellectual property by the companies that develop it. Dr. Dyer will testify that (1) the combination of process steps and the sequence of those steps; (2) the combination of recipes associated with individual steps; and (3) the combination of tools used to perform the steps are each highly valuable trade secrets. The complete combination of steps, recipes, and/or tools described in any particular document is a valuable trade secret, along with at least the subsets of steps, recipes, and/or tools described in the government's forthcoming bill of particulars. He will testify that he is aware that such information is the result of large investments in time, people, and money, and companies carefully consider how such information is handled to maximize its value to the company.

Dr. Dyer will testify that the process steps, sequence, recipe information, and tooling information in Trade Secret 1-8 is the culmination of many successive generations of technology development— representing years of a complex engineering development and refinement by teams of engineers to develop and implement process technology. Each generation of DRAM builds on the development of preceding generations to make the DRAM circuits incrementally smaller and to create electrical devices that pack more digital storage into progressively smaller areas of a semiconductor chip. Each generation of process technology is the result of substantial investment—typically ranging from many hundreds of millions of dollars to upwards of a billion dollars for the process R&D along, when that R&D has a prior technology base to build on.

Many aspects of a preceding-generation process technology are carried over and only those steps that can no longer meet the scaling requirements are typically changed. Even so, developing a new technology from a previous generation and making it ready for manufacturing involves dozens of scientists and engineers with advanced degrees and hundreds of other engineers and technicians, working over the course of years and requiring extensive use of billion-dollar wafer fabs and thousands of silicon wafers. The process-development process involves starting with the previous technology, identifying those processes that need to be improved or changed in order to scale the DRAM size down, performing feasibility test by running abbreviated short-flow process vehicles, demonstrating the targeted structure, satisfying basic electrical requirements, demonstrating circuit functionality, ramping product yield, and demonstrating operational lifetime reliability, among other engineering efforts. The effort to design, acquire, and/or select a tool for an individual process step can involve a substantial investment of time and resources. Given the immense complexity, it is extremely unlikely that two independently developed process flows would have even remotely similar steps, recipes, or tools.

Dr. Dyer will testify that the information is Trade Secrets 3 and 4 is further the result of a sophisticated and complex work in the field of device physics. Developing ion-implant conditions involves incorporating the learning and development from previous technology nodes. Engineers then conduct additional simulations and experiments to arrive at a set of conditions that satisfy the device requirements of the DRAM technology under development. Engineers conduct computer modeling of implant conditions to determine how they affect device operation, and continually verify those conditions by performing the implants on wafers and measuring their actual effect. This process typically involves continually tweaking the implant conditions throughout the development cycle to get optimal device performance. There is generally not just one set of implant conditions that could meet the requirements, and the specific set of conditions arrived at depends on the particular starting point and the development path taken. As such, it is extremely unlikely—if not impossible—for two independent developments to arrive at the same or very similar implant conditions.

Dr. Dyer will testify that the design-rule information in Trade Secret 5 is the result of many generations of process-technology development for a functional, high yielding, and reliable circuits. The 25 nm design rule document represents the culmination of all previous design rule development in prior technology nodes. The resources required to produce such a combination of design rules is commensurate with the cost of developing all of the preceding technology nodes and up to the latest node since the ground rule information is derived from know-how gained in developing those technologies.

Dr. Dyer may testify that the process technology required to create DRAM is so refined and complex that, for the past few decades companies seeking to enter the DRAM manufacturing business generally do not seek to independently develop it. Instead, they look to acquire legacy DRAM technology from an existing manufacturer either by buying the existing DRAM company or by licensing the technology from a company willing to sell it. Either way, the new DRAM entrant obtains the technology by getting the detailed documentation of the technology and access to the engineers who will be tasked to install and maintain the technology in their facility as needed.

Dr. Dyer will testify that an actual or would-be competitor who came into possession of Trade Secrets 1-8 (separately or collectively) would be able to substantially accelerate the development of DRAM process technology by avoiding a large majority of the substantial costs associated with developing the technology independently or acquiring it legitimately. Moreover, by avoiding the substantial investment required to legitimately develop or acquire the technology, a company that misappropriated the Trade Secrets would be able to undercut DRAM competitors in the marketplace, who would need to price their DRAM products at a point that allows recoupment of the investment in research and development. Because DRAM is by and large a commodity product, a company that is able to avoid incurring research and development costs could eventually drive its competitors out of business.

Dr. Dyer's opinions about the value of Trade Secrets 1-8 (and any subparts identified in the government's forthcoming bill of particulars) is substantially the same whether the trade secrets are considered separately or collectively. The more information a competitor or would-be competitor acquired, the more development they would be able to avoid, along with the costs associated with an independent development for developing process technology and selecting tools.

Dr. Dyer's opinions with regard to the value of Trade Secrets 1-8 to a would-be or actual competitor is based on his experience in the field of semiconductors and DRAM. Because Dr. Dyer has participated in the development of DRAM and DRAM process technology, he is able to opine on how a competitor could use research and development information to develop DRAM and DRAM process technology.

E. Trade Secrets 1-8 are Trade Secrets under 18 U.S.C. § 1839

Dr. Dyer will attend the trial in this case and will listen to testimony regarding the measures Micron employed to protect the information in Trade Secrets 1-8. Based on that testimony, Dr. Dyer may testify that Micron took precautions that were reasonable in the industry. That testimony would be based on his extensive experience in the field of semiconductor process technology and DRAM, and experience with companies that develop DRAM. Depending on his opinions regarding the measures taken to protect Trade Secrets 1-8, Dr. Dyer may testify that each of Trade Secrets 1-8 (along with any sub parts identified in the government's forthcoming bill of particulars) are Trade Secrets under 18 U.S.C. § 1839(3).

III. The Project M DRAM Development Used Micron's Information—Including Information Identified as Micron Trade Secrets—to Develop DRAM Technology

A. Dr. Dyer's Understanding of Rexchip and Elpida and the Micron Acquisition

Dr. Dyer will testify that he understands that Micron came to acquire trade secrets originally owned by Rexchip and Elpida. Dr. Dyer will testify that he understands that proprietary information, including trade secrets, originally owned by Rexchip or Elpida came to belong to Micron after Micron acquired Rexchip (which itself was a joint venture between Elpida and Powerchip). Elpida developed new technologies at their E300 facility and transferred it to Rexchip's R1 facility for mass production. After Micron acquired Elpida and Rexchip, Elpida E300 was renamed Micron Fab 15 and Rexchip R1 was renamed Micron Fab 16. Under Micron management, the two sites continued their usual roles in developing, transferring, and mass producing DRAM technologies. Technologies developed at Elpida E300 (Micron Fab 15) and transferred to Rexchip R1 (Micron Fab 16) included the 25 nm technology. In the technology transfer activity, Elpida (Micron Fab 15) would provide detailed documentation, engineering support, and training to Rexchip (Micron Fab 16).

The information upon which Dr. Dyer primarily relied on for the understandings expressed in this section are listed in Exhibit 4 § A.[1]

B. Appropriation of Micron's Process

Dr. Dyer may testify that the Project-M development used Micron's process technology as the foundation/starting point for the entire Project-M process development. Instead of developing process technology from scratch, the Project-M team started with a virtually complete description of DRAM process flow and recipe information for three generations of Micron technology: 90 series (25 nm), 100 series (20 nm), and 110 series (1 xnm).

The Project-M team met in December 2015 and started with an exact copy of Micron's recent process flow, as described in the trade-secret documents describing the Rexchip 25nm Process Flow. That flow included a detailed description of Rexchip's 25 nm process flow, along with a more recent update to that flow. The documents reflect that the Project M Team then analyzed—step by step—how to leverage UMC's existing logic tools to accomplish Micron's process steps, and what process steps were new for UMC. Instead of developing process steps, process recipes, and sequencing process steps from scratch, UMC had that information from Micron, and engaged in an effort to fit Micron's manufacturing process into UMC's environment with minimal cost, for example, by adapting UMC's fabrication equipment, or procuring new equipment that UMC did not already have.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § B.

C. Project M's Three-Generation Strategy

Dr. Dyer will testify that the longer-term strategy for Project M was to pursue a three-generation technology strategy that would allow Project M to quickly catch up to the state-of-the art technology manufactured by the big-3 existing DRAM companies. At the outset, the Project-M team—based on its knowledge of Micron's technology—decided to pursue 25 nm technology that it code-named "F32." The development plans included a rapid progression from F32 to a 20 nm technology codenamed "F32S." The Project M team planned to eventually leverage those developments to move to 1x nm technology that would be much closer to the by-then existing state-of-the art technology of other DRAM manufacturers.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § C.

[1] Dr. Dyer provided the material in Exhibit 4 to the United States.

D. Project M's Selection of a Memory Cell Layout

Dr. Dyer will testify that, in order to more quickly catch up to competitors, and based in part on their access to Micron's Trade Secrets 1-8, the Project M team decided to implement a feature of Micron's 110 series technology in Project-M's F32 design, and all subsequent designs. Specifically, the Project-M team recognized that starting with 3x2 DRAM cell architecture (used in Micron's 110 series and by DRAM manufacture Samsung) instead of a 2x3 cell architecture (used in Micron's 90 and 100 series DRAM) would allow UMC/Jinhua to avoid row-hammer issues Micron encountered as it scaled down from its 100 series to its 110 series, and that eventually led Micron to switch to a 3x2 cell architecture for the 110 series. Moving to a 3x2 architecture in its early generation technology would allow UMC/Jinhua to more rapidly catch up to other DRAM competitors in the field as it progressed to 1x nm technology and beyond. By implementing features found in later generations of Micron's technology, UMC could build a manufacturing line once that would be capable of manufacturing three generations of technology, without incurring the costs like those that Micron did in evolving its technology from 25 nm to 1x nm.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § D.

E. Comparison of Micron Process Flows to Project M Process Flows Over Time

Dr. Dyer will testify that he reviewed the development and progression of UMC's manufacturing process starting from December 2015 through the transfer of the technology to Jinhua in September 2018. Dr. Dyer found a continuous development, with evolutionary alterations, that started from the Micron/Rexchip process. At no time in the development process did Dr. Dyer observe any abrupt deviations or changes to indicate the removal of the Micron foundation upon which Project-M process was built and eventually transferred to Jinhua in the September 2018 technology transfer package. Dr. Dyer performed detailed comparisons of the Micron trade secrets and process flows to the Project-M process flow as it existed in December 2015, December 2016, and September 2018.

Dr. Dyer will present those comparisons at trial via demonstratives that compare Micron's process technology (steps, sequences, recipes, and tools) to the Project-M process flow on a step-by-step basis. Those comparisons will show how the Project-M implementation of Micron's process evolved over time in a predictable, logical way. Dr. Dyer will testify that by the time the Project-M process flow was finalized in September 2018, the overall combination of process steps and the sequence of those steps, as the Project-M team originally copied them from Micron's documents, was largely intact for key process modules. Many of the steps that were added or deleted by Project M were largely inconsequently steps (such as cleaning steps), or appear to be the result of the expected engineering effort that must be undertaken to transfer (or here, copy) technology from one semiconductor fab to another. Dr. Dyer will testify based on

his extensive training and experience in the development of DRAM process technology that it is extremely unlikely that an independent technology development effort would have arrived at process flow as similar to Micron's as that in the 2018 Technology Transfer Package.

Many of the changes in process recipes (from the original copy of Micron to the September 2018 technology transfer package) are the types of changes that one would expect when transferring an existing process technology to a new fab. A number of process steps, however, included specific, detailed parameters that were either unchanged or only slightly changed from Micron's technology. Finally, the changes in tooling from Micron's process flow to the Project M process flow reflect the normal tooling changes that might exist between different fabs, and reflect Project M's overall strategy to implement Micron's process flow using as much of UMC's existing tooling as possible.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § E. The documents cited in Exhibit 4 § E allow for a relatively complete comparison of the Micron process flow and the Project-M process flow, as the process M process flow existed at various points in time. At trial, Dr. Dyer will present side-by-side comparisons of the process flows described by those documents. An example of the general type of demonstrative Dr. Dyer may use at trial to compare Micron and Project M process flows is attached as Exhibit 5.[2] That exhibit compares Micron's process flow for creating buried wordlines in its 25 nm technology with the process flow for buried wordlines in the September 2018 Technology Transfer Package.

F. Process Comparison and Evolution: Buried Wordline and Capacitor Formation

Dr. Dyer will testify that the he observed the highest degree of similarity between the Micron and Project M process flows as they concern the manufacturing of DRAM capacitors and buried wordlines. The capacitors and buried wordlines are the most challenging aspects of manufacturing DRAM, that separate a DRAM manufacturing from, for example, a logic manufacturer like UMC.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § F.

G. Process Comparison and Evolution: Logic Device Formation

Dr. Dyer will testify that he observed a high degree of similarity indicative of copying of Micron's information by the Project-M team with respect to the following aspects of the process technology: (1) well and channel implants; (2) CMOS gate formation; and (3) spacer and junction implants. Ion implant processes have an array of parameters that define each step with

[2] Dr. Dyer provided the material in Exhibit 5 to the United States.

many degrees of freedom. It would be highly unlikely for ion-implant processes developed independently at different fabrication facilities to match each other to any significant degree. The degree to which the various ion implant steps match between two fabrication sites at a particular point in the development cycle would be a good indication of the degree of copying taking place between those sites.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § G.

H. Process Comparison and Evolution: Use of Micron 1x nm Technology to Implement the Project M 3x2 cell array

Dr. Dyer will testify that the Project-M team used information from Micron's 1x nm process, including information from Trade Secrets 7 and 8, to develop the technology requirement to implement a 3x2 cell array—which Micron implemented in its 3x2 DRAM—in the Project M DRAM. Dr. Dyer observed similarities indicative of copying from Micron's 110 series technology in at least the following process components: (1) the shallow trench isolation (STI) pinch-off process, (2) the bitline contact (BC) process, and (3) the storage node contact (SC process).

The change to a 3x2 cell drives tighter spacing between active areas in the memory cell array and these tighter gaps require an insulator deposition process that can fill them without voids, seams, or other weaknesses of the material filling the isolation trenches.

Because the active areas of the 3x2 cell are staggered instead of lined-up as they are in the 2x3 cell of Elpida's 25nm technology, the structures that are built on top of the active areas such as the bitline contacts and capacitors contacts need to be staggered instead of line up as well.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § H.

I. Process Comparison and Evolution: Interconnects (Micron 1x)

Dr. Dyer will testify that the Project M team used information from Micron's 1x nm process, including information from Trade Secrets 7 and 8, to develop and implement the processes to create interconnects in the Project M DRAM. Dr. Dyer observed similarities indicative of copying from Micron's 110 series technology in at least the following process components: (1) the back end of line process sequence (BEOL), and (2) the formation of local interconnects.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § I.

J. Comparison of Product Designs

Dr. Dyer will also testify that, in addition to using Micron's process technology, including as described in Trade Secrets 1-8, UMC/Jinhua used a DRAM design sourced from a company called Ultra Memory Inc. (UMI). UMI's design appears to be very similar to a Micron design that UMI obtained through a relationship with Powerchip.

Dr. Dyer will testify about the connection that must exist between a DRAM circuit design/layout and DRAM process technology. A DRAM circuit designer must design within the constraints of what a particular semiconductor fab can build. If the designer does not, she will design DRAM circuitry that the foundry cannot build. As such, a typical DRAM development would begin with specifications from the fabrication line, and the designers would design to fit within that process. The Project-M development, however, did not follow that normal process. Instead, the Project-M development documents indicate that the Project-M team was able to procure a version of an off-the-shelf design from the DRAM design house UMI early on in the project. The Project-M team used that design to essentially spec the requirements of the fabrication process they were developing. To the extent the UMI design was previously fabricated in Micron/Rexchip/Elpida fab, use of the Micron process technology would be especially valuable for Project-M, since it would have been known that the UMI design could be manufactured with Micron's process technology described in Trade Secrets 1-8.

Project M also had possession of a similar Elpida 4GB design. The Elpida design closely resembled the design provided by UMI in the sense amplifier circuits (the UMI design is slightly larger) and use the same memory cell dimensions.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § J.

K. Opinions Regarding Process Changes Driven by the Change from 2x3 to 3x2 layout

Dr. Dyer will testify that the choice between a 3x2 DRAM cell architecture and a 2x3 cell architecture is primarily one related to the DRAM circuit design and layout. Except for some modifications, process technology intended to fabricate a 2x3 DRAM cell array could also be utilized to fabricate a 3x2 DRAM cell array. Micron itself changed to a 3x2 architecture for its 1x nm process, as indicated in Trade Secret 7.

A 3x2 cell architecture drives some changes in process (as compared to the process to manufacture a 2x3 array), such as bitline contacts, capacitor contacts (layout change), tighter active areas (requiring spin-on di-electrics for filming), and some other relatively minor differences.

In other ways the change to 3x2 makes the fabrication easier. For example, the relaxed wordline pitch makes the buried wordlines easier to form and less prone to row hammer issues which would have to be dealt with one way or another. In the long run as the technology is scaled, the 3x2 cell would represent a significant facilitation of the fabrication of functional DRAM products, as the Micron 110 series process traveler documents spells out.

Dr. Dyer's opinions with regard to process changes required to change from 2x3 to 3x2 are based on his education and extensive knowledge in the field of DRAM process integration. Dr. Dyer also compared the changes that Micron made to its flow to change from a 2x3 node to a 3x2 node in its 110 series DRAM, along with the changes UMC made to Micron's process flows to create a 3x2 node.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § K.

L. Use of Key People

Dr. Dyer will testify based on his training, experience, and common sense that it would be advantageous for Project M to hire Micron employees to work on Project M, as compared to employees from other DRAM companies. Micron employees would be familiar with Micron's process technology, and better able to copy, reference, or otherwise misappropriate the information to the advantage of Project M.

Dr. Dyer will also testify based on his exhaustive review of Micron documents that many of the employees who left Micron to joint Project M, including JT Ho, worked extensively on transfers of process technology from Micron Fab 15 (the old Elpida E300 development fab) to Micron Fab 16 (the old Rexchip R1 fab). Those employees, therefore, had extensive experience in the non-trivial engineering effort required to take process technology from one fab and implement it—with the necessary changes—at another fab. Those employees thus had the necessary background knowledge and engineering insight to anticipate problems and know what solutions are likely to be most effective in resolving them.

The information upon which Dr. Dyer primarily relied on to form the opinions expressed in this section are listed in Exhibit 4 § L.